

Application No.: 10/820,601

Docket No.: JCLA12197-R

In The Claims:

Claims 1-8 (canceled)

Claim 9. (currently amended) A semiconductor device, comprising:

a substrate;

a gate structure on said substrate, said gate structure including a gate dielectric layer on said substrate and a gate conductive layer on said gate dielectric layer;

an oxide spacer on a sidewall of said gate structure;

a spacer on said oxide spacer;

a source/drain region in said substrate besides said gate structure and said spacer; and

an offset oxide layer on said substrate and in a portion of said source/drain region, wherein said offset oxide layer having a bottom surface below a bottom surface of said gate dielectric layer is ~~apart-separated~~ apart-separated from said gate structure ~~and adjacent to by~~ said spacer and said oxide spacer.

Claim 10. (original) The device of claim 9, wherein a material of said oxide spacer includes silicon oxide.

Claim 11. (original) The device of claim 9, wherein a material said spacer includes silicon nitride.

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Claim 12. (original) The device of claim 9, wherein said oxide spacer has an etching selectivity relative to said spacer.

Claim 13. (original) The device of claim 9, further comprising a source/drain extension region below said oxide spacer and adjacent to said source/drain region.

Claim 14. (original) The device of claim 9, wherein a width of said oxide spacer is not larger than a width of said spacer.

Claim 15 (currently amended) A semiconductor device on a substrate, comprising:
a gate structure on the substrate;
a spacer over the sidewall of the gate structure;
a heavily doped source/drain region in a portion of the substrate exposed by the gate structure and the spacer; and
an offset oxide layer on the heavily doped source/drain region, wherein the offset oxide layer has a bottom surface below a bottom surface of the gate dielectric layer and the offset oxide layer is separated from the gate structure by the spacer.

Claim 16 (previously presented) The device of claim 15 further comprising an oxide layer located between the spacer and the gate structure and between the spacer and the substrate.

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Claim 17 (previously presented) The device of claim 16, wherein the offset oxide layer is an extension portion of the oxide layer and the thickness of the offset oxide layer is larger than that of the oxide layer.